STRUCTURE AND METHOD FOR SUPPRESSING SUB-THRESHOLD LEAKAGE IN INTEGRATED CIRCUITS

ABSTRACT

Techniques for reducing leakage power in the transistors of integrated circuits are provided. Suppressing sub-threshold leakage techniques can be applied to memory cells that drive the gates of the transistors, memory cells that drive the sources of the transistors, and level shifters that drive the gates of the transistors. In these techniques, an appropriate gate to source voltage (V_{GS}) can be applied to a transistor in its off state. Of importance, this V_{GS} can under-drive the transistor, which significantly reduces the sub-threshold leakage of that transistor. These techniques fail to affect a transistor in its on state, thereby ensuring that high speed performance of the integrated circuit can be maintained.